WHAT IS CLAIMED IS:

1. A method, comprising:

configuring a plurality of timers with interrupt event arrival rates;

measuring a rate of arrival of one or more interrupt events; and

asserting an interrupt, in response to the measured rate of arrival of the one or more interrupt events being lower than the interrupt event arrival rates configured in the plurality of timers.

2. The method of claim 1, wherein the one or more interrupt events are arrivals of packets, and wherein the interrupt event arrival rates are different for at least two timers, and the measuring is performed with the at least two timers.

3. The method of claim 1, further comprising:

in response to asserting the interrupt, restarting the plurality of timers.

4. The method of claim 1, wherein the configuration further comprises:

initializing the plurality of timers with countdown time periods, wherein a countdown time period measures a period of time; and

initializing the plurality of timers with a reset criteria, wherein a first reset criterion for a first timer indicates a first number of interrupt events that are to be received by the first timer within a first countdown time period for the first timer to be restarted.

5. The method of claim 1, wherein the configuration of the plurality of timers regulates a latency of an arriving interrupt event in generating interrupts.

6. The method of claim 1, wherein the configuration, measurement, and assertion result in one interrupt being generated for a plurality of arriving events.

7. The method of claim 1, wherein the configuration, measurement, and assertion are performed by an interrupt generator, including an Input/Output controller, wherein the interrupt generator is coupled to a computational device, wherein the computational device is capable of receiving the one or more interrupt events to result in interrupts at one rate at which the computational device can process the interrupts without decreasing performance of other functions of the computational device.

8. The method of claim 1, wherein the configuration and assertion are performed by an interrupt moderator included in a computational device, wherein the interrupt moderator includes the plurality of timers, wherein an interrupt moderation level of a first timer is different from an interrupt moderation level of a second timer.

9. The method of claim 1, wherein the configuration of the plurality of timers is based on a consideration of possible load on a processor based on a level of possible interrupts to the processor and a desired latency of the arriving interrupt events.

10. An interrupt generator, wherein the interrupt generator is capable of being coupled to a computational device, the interrupt generator comprising:

a plurality of timers capable of being configured with interrupt event arrival rates; and

an interrupt moderator coupled to the plurality of timers, wherein the interrupt moderator is capable of measuring a rate of arrival of one or more interrupt events, and wherein the interrupt moderator is capable of asserting an interrupt in response to the measured rate of arrival of the one or more interrupt events being lower than the interrupt event arrival rates configured in the plurality of timers.

11. The interrupt generator of claim 10, wherein the interrupt generator is an I/O controller, wherein the one or more interrupt events are arrivals of packets, and wherein the interrupt event arrival rates are different for at least two timers.

12. The interrupt generator of claim 10, wherein in response an assertion of the interrupt, the interrupt moderator is capable of restarting the plurality of timers.

13. The interrupt generator of claim 10, wherein the interrupt moderator further comprises:

countdown time periods, wherein the interrupt moderator is capable of initializing the plurality of timers with the countdown time periods, wherein a countdown time period measures a period of time; and

reset criteria, wherein the interrupt moderator is capable of initializing the plurality of timers with the reset criteria, wherein a first reset criterion for a first timer indicates a first number of interrupt events that are to be received by the first timer within a first countdown time period for the first timer to be restarted.

14. The interrupt generator of claim 10, wherein a configuration of the plurality of timers is capable of regulating a latency of an arriving interrupt event in generating interrupts.

15. The interrupt generator of claim 10, wherein one interrupt is generated for a plurality of arriving interrupt events..

16. The interrupt generator of claim 10, wherein the interrupt generator is an Input/Output controller, wherein the computational device is capable of receiving the one or more interrupt events to result in interrupts at one rate at which the computational device is capable of processing the interrupts without a decrease in the performance of other functions of the computational device.

17. The interrupt generator of claim 10, wherein the interrupt moderator is included in the computational device, wherein the interrupt moderator includes the

plurality of timers, wherein an interrupt moderation level of a first timer is different from an interrupt moderation level of a second timer.

18. The interrupt generator of claim 10, wherein the configuration of the plurality of timers is based on a consideration of possible load on a processor of the computational device based on a level of possible interrupts to the processor and a desired latency of the arriving interrupt events.

19. A system, comprising:

a computational device;

a data storage coupled to the computational device;

a data storage controller to manage Input/Output access to the data storage, wherein the data storage controller is coupled to the computational device;

an interrupt generator, wherein the interrupt generator is capable of being coupled to the computational device;

a plurality of timers capable of being configured with interrupt event arrival rates, wherein the plurality of timers is coupled to the interrupt generator; and

an interrupt moderator coupled to the plurality of timers, wherein the interrupt moderator is capable of measuring a rate of arrival of one or more interrupt events, and wherein the interrupt moderator is capable of asserting an interrupt in response to the measured rate of arrival of the one or more interrupt events being lower than the interrupt event arrival rates configured in the plurality of timers.

20. The system of claim 19, further comprising:

countdown time periods, wherein the interrupt moderator is capable of initializing the plurality of timers with the countdown time periods, wherein a countdown time period measures a period of time; and

reset criteria, wherein the interrupt moderator is capable of initializing the plurality of timers with the reset criteria, wherein a first reset criterion for a first timer

indicates a first number of interrupt events that are to be received by the first timer within a first countdown time period for the first timer to be restarted.

21. The system of claim 19, wherein the interrupt generator is an Input/Output controller, wherein in response to the assertion of the interrupt, the interrupt moderator is capable of restarting the plurality of timers.

22. An article of manufacture, wherein the article of manufacture is capable of causing operations, the operations comprising:

configuring a plurality of timers with interrupt event arrival rates;

measuring a rate of arrival of one or more interrupt events; and

asserting an interrupt, in response to the measured rate of arrival of the one or more interrupt events being lower than the interrupt event arrival rates configured in the plurality of timers.

23. The article of manufacture of claim 22, wherein the one or more interrupt events are arrivals of packets, and wherein the interrupt event arrival rates are different for at least two timers, and the measuring is performed with the at least two timers.

24. The article of manufacture of claim 22, the operations further comprising:

in response to asserting the interrupt, restarting the plurality of timers.

25. The article of manufacture of claim 22, wherein the configuration further comprises:

initializing the plurality of timers with countdown time periods, wherein a countdown time period measures a period of time; and

initializing the plurality of timers with reset criteria, wherein a first reset criterion for a first timer indicates a first number of interrupt events that are to be received by the first timer within a first countdown time period for the first timer to be restarted.

26. The article of manufacture of claim 22, wherein the configuration of the plurality of timers regulates a latency of an arriving interrupt event in generating interrupts.

27. The article of manufacture of claim 22, wherein the configuration, measurement, and assertion result in one interrupt being generated for a plurality of arriving interrupt events.

28. The article of manufacture of claim 22, wherein the configuration, measurement, and assertion are performed by an interrupt generator, including an Input/Output controller, wherein the interrupt generator is coupled to a computational device, wherein the computational device is capable of receiving the one or more interrupt events to result in interrupts at one rate at which the computational device can process the interrupts without decreasing performance of other functions of the computational device.

29. The article of manufacture of claim 22, wherein the configuration and assertion are performed by an interrupt moderator included in a computational device, wherein the interrupt moderator includes the plurality of timers, wherein an interrupt moderation level of a first timer is different from an interrupt moderation level of a second timer.

30. The article of manufacture of claim 22, wherein the configuration of the plurality of timers is based on a consideration of possible load on a processor based on a level of possible interrupts to the processor and a desired latency of the arriving interrupt events.